

What Is Claimed Is:

1 1. A method of processing signals of a timing controller
2 of a liquid crystal display module, comprising the steps of:

3 (a) receiving a data enable signal DE which has a vertical
4 blank period;

5 (b) generating a gate clock signal CPV which has a plurality
6 of gate clock cycles C1-Cn;

7 (c) generating a plurality of gate-on enable signals OE
8 simultaneously according to the plurality of gate clock cycles
9 C1-Cn of the gate clock signal CPV; and

10 (d) generating start vertical signals STV before the end
11 of the vertical blank period VB and after at least a gate clock
12 cycle C1 during the vertical blank period VB.

1 2. The method as claimed in claim 1, wherein in the step
2 (c), start vertical signals STV are generated after at least a
3 third cycle C3 during the vertical blank period VB.

1 3. The method as claimed in claim 1, after the step (d)
2 further comprising a step of:

3 pausing outputting CPV, STV, and OE till the end of the
4 vertical blank period VB.

1 4. The method as claimed in claim 1, wherein the start
2 vertical signals STV includes:

3 a first start vertical signal STV1, for determining a start
4 scan location of a frame; and

5 a second start vertical signal STV2, for offsetting flicker
6 and display brightness of the liquid crystal display .

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- 1 5. The method as claimed in claim 1, wherein the start
- 2 vertical signals STV uses only a first start vertical signal STV1
- 3 to determine a start scan location of a frame;

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